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For Immediate Release

***Technical Highlights:***

***2024 IEEE Electronic Components and Technology Conference***

The 74th annual [IEEE Electronic Components and Technology Conference (ECTC)](https://www.ectc.net/index.cfm) will take place May 28-31, 2024 at Denver’s Gaylord Rockies Resort & Convention Center. It is the world’s leading forum for unveiling, discussing and exhibiting the latest advances in microelectronics packaging and component science and technology. More than 1,500 scientists, engineers and businesspeople from 20+ countries are expected to attend, along with more than 115 exhibitors.

Packaging- and component-related technologies are key to continuing the advances in electronics we have come to expect, because it has become much more difficult and expensive to further scale down transistor feature sizes, already measured in nanometers. Instead, the electronics industry is looking at a number of alternative approaches which will be highlighted at IEEE ECTC 2024. These topics include chips in 2.5/3D package configurations; heterogeneous integration, or the integration of multiple chips or dies with diverse functionalities into a single package; the use of co-packaged photonic technologies for faster, more energy-efficient interconnections within chip modules; ways to test for and increase the reliability of these highly integrated systems and their novel architectures; and many related issues.

This Tip Sheet describes noteworthy technology themes and papers from IEEE ECTC 2024.

1. **Heterogeneous Integration and 2.5/3D Circuits**

**A Complete Computer System on a Tiny Substrate for Ultra-Compact Edge Computing:** IBM researchers will detail a high-throughput, manufacturable, heterogeneous integration-based chiplet packaging process, for use in sensor data acquisition and secure communications in military, commercial and consumer applications. The process makes it possible to build a complete computer system with a wide range of functionality on a tiny substrate (<1mm2), comprising a 32-bit processor, memory, analog I/O with built-in temperature and chemical sensors, energy-harvesting power source, and operating system software. The process incorporates wafer-to-wafer (W2W) transfer, with integrated Si and/or III-V optical photovoltaic/photodiode cells fabricated on Si carriers.

To demonstrate the packaging process, the researchers built heterogeneous chips thinned to 50-100 μm, with lateral dimensions of several hundred microns, separated by ~20 μm gaps, and with 10-20 μm-diameter copper pillars. They say the process enables reliable and high-throughput system-on-a-carrier packaging with a diverse set of CMOS, GaN and GaAs chip technologies. **(Paper 34.6, “*Ultra-Compact Computing at the Edge Involving Unobtrusively Small Sub-Millimeter Heterogeneous Integration Packaging*,” F. Libsch et al, IBM)**

**Advanced Packaging for AI Hyperscale Computing**: Given the growth in large language models (LLMs) for artificial intelligence (AI) applications, a single neural network may now contain billions of parameters for computation. That number is expected to increase further at an unprecedented rate. For higher-performance, more energy-efficient neural network computing, more processor and memory dies need to be integrated in a single package. However, fabricating these integrated systems is difficult and costly. It is also challenging to increase memory bandwidth, due to the memory bottleneck arising from the relatively slow bandwidth of off-chip memory, and from the excessive energy consumption needed for frequent data access.

A joint research team from KAIST-ETRI-AMKOR will describe a proposed advanced packaging solution they used to build a AI hyperscale processor unit (HPU) test vehicle, consisting of a pair of neural processor unit (NPU) chiplets and eight high-bandwidth memory 3 (HBM3) chiplets. The dual-NPU chiplets achieved peta-scale performance through energy-efficient tensor cores optimized for AI computation. All 10 chiplets were integrated on a large-scale RDL (redistribution layer) interposer and package substrate. High-density interconnect was used between the NPU and HBM to enable near-TB/s inter-chiplet bandwidth, allowing most data to be retrieved near the NPU for faster performance and greater energy-efficiency. The researchers will detail their overall design methodology and also will discuss thermal integrity simulations. **(Interactive Presentation #38.5, “*The Energy-Efficient 10-Chiplet AI Hyperscale NPU on Large-Scale Advanced Package*,” J. Yoon et al, KAIST/ETRI/Amkor Technology)**

**Comparing Various Backside Power Delivery Schemes:** As semiconductor technology scaling continues, it becomes more challenging to fabricate low-loss power delivery networks (PDNs). Backside power delivery architectures have been introduced and are being developed for advanced nodes to mitigate the increasing risks of both static IR-drop (SIR) and dynamic voltage drop (DvD) that occur with conventional front-side PDNs. Samsung researchers will describe how three different backside power delivery schemes under development industry-wide compare to front-side power delivery performance: 1) through-silicon vias; 2) buried power rails; and 3) back-side direct contacts. These differ in how the backside power delivery network is connected to active devices. The Samsung researchers also will describe the importance of system-level analysis and design co-optimization between the on-chip PDN and the packaging. **(Paper 22.3, “*System-Level Analysis and Design Optimization of Back-side Power Delivery Network For Advanced Nodes*,” K. Song et al, Samsung)**

**Novel Stacking Process:** Sony researchers will show how a successful electrical connection through three layers can be achieved, paving the way toward a process for three-layer stacked 3D heterogeneous integration. They will describe a chip-on-wafer-on-wafer (CoWoW) process, involving a three-layer vertically stacked structure comprising face-to-back (F2B), chip-on-wafer (CoW), and face-to-face (F2F) wafer-on-wafer (WoW) using 6 µm-pitch copper-to-copper (Cu-Cu) connections. Bowing of the top chip was controlled to achieve void-free CoW bonding, and CoW bonding strength was simulated using elastic strain energy testing. Excellent 6 µm-pitch Cu-Cu connections of F2B CoW were achieved, both at the center and at the edge of the chip, as well as F2F WoW. Additionally, the 6 µm-pitch Cu-Cu connections using CoWoW exhibited high reliability in stress-induced voiding and electromigration tests. **(Paper #2.4, “*Novel Three-Layer Stacking Process With Face-to-Back CoW 6 µm-Pitch Hybrid Bonding*,” A. Urata et al, Sony)**

**An Ideal Assembly Platform for 2.5D/3D Integration:** Silicon carrier wafers with inorganic bond/debond layers offer sub-micron total thickness variation (TTV), excellent thermal/mechanical stability, and compatibility with high temperatures and with all silicon wafer tools and processes. As such, they can serve as an ideal assembly platform, enabling new opportunities for 2.5D/3D integration.

Intel researchers will describe an infrared (IR) laser debond technology that uses inorganic thin films to control laser release from such silicon carrier wafers. They will also discuss how they integrated it into high-density interconnect process flows. They demonstrated transfers of backend (BE) metal layers, 3-µm pitch hybrid-bond interconnects (HBI), and singulated chiplets from silicon carrier wafers to silicon receiver wafers without damage to any transferred layers, chiplets, or the silicon carrier. They also demonstrated damage-free IR laser debond of an organic inter­poser with two redistribution layers (RDL) with up to 333 lines/mm, fabricated using Intel’s Zero-Misalignment-Via (ZMV) process technology on a silicon carrier wafer. An optical model was used to predict multi-layer absorption and transmission, and to demonstrate the benefits of a shield layer. **(Paper #9.5, “*IR Laser Debond From Silicon Carrier Wafers With Inorganic Thin Film Release Layers For High-Density 2.5D­­­ and 3D Integration*,” T. Sounart et al Intel)**

**A Demonstration of a Hybrid Bonded 3D Architecture with Applications in CMOS Image Sensors:** 3D integration, where multiple device layers are stacked vertically, enables the integration of multiple functions in a compact space, improving performance and reducing power consumption. Hybrid bonding (HB), also known as Cu-Cu direct bonding, provides a high-density, low-resistance interconnection between two bonded wafers. Through-silicon vias (TSVs) also play a crucial role in 3D integration by providing a pathway for efficient signal transfer and power distribution between the vertically stacked layers. For CMOS image sensors, combining hybrid bonding with high-density TSV arrays could facilitate the integration of various functionalities with unparalleled precision and compactness, such as image sensor arrays, signal processing circuits, and memory elements.

Researchers from CEA-Leti will describe various test vehicles they built to explore this approach, ultimately resulting in a three-layer demonstrator with both standard pitch (6 µm) and fine pitch (4 µm) and with two Cu-Cu hybrid bonding interfaces (one face-to-face and one face-to-back) combined with high-density TSVs (10 µm height, 1 µm diameter). After fabrication, characterizations of the structures (FIB-SEM cross-sections) verified that the entire 3D stacked structure had good metal connection at the HB and TSV interfaces. For electrical characterization, different types of Kelvin and Daisy Chain structures were tested. The results for the Kelvin structures showed a median resistance of just a few ohms, and a >80% yield. Those results were confirmed by electrical measurements on the Daisy Chain structures. The researchers say that after this demonstration of three-layer functionality, the next step will be to implement the 3D technology in a functional advanced CMOS image sensor. **(Paper #8.2, “*3-Layer Fine Pitch Cu-Cu Hybrid Bonding Demonstrator With High Density TSV For Advanced CMOS Image Sensor Applications*,” S. Nicolas et al, Grenoble Alps Univ./CEA-Leti)**

**A Dry Film Resist for RDL Panels:** Advanced packaging solutions for 3D, 2.5D, 2.1D and fan-out structures require fine-pitch redistribution layers (RDL) – typically less than 2 µm wide – to distribute a large number of input/output connections within a small space. RDLs made from large square panels instead of traditional circular wafers are growing in appeal because they allow for highly efficient use of the panel area, enabling efficient, high-volume production. However, equipment limitations and potential warpage make it challenging to fabricate panel-format RDLs, because of the need to apply photoresist material across a large panel with good thickness uniformity. Liquid resists offer high resolution and are widely used in high-quality wafer manufacturing, but they are difficult to apply to large panels. Dry film resists, meanwhile, offer lower resolution but are less expensive, easier to use and more suitable for large panel applications.

A team from Resonac Corp. will describe a new negative-tone dry film resist with a high 1 μm resolution (aspect ratio 6.0) on wafers, and 1.5 μm resolution (aspect ratio 4.0) on an ABF substrate panel. (ABF substrates are insulating layers designed to allow specific interconnections.) The new material can form copper wiring with a 2 µm pitch on wafers, and a 3 µm pitch on ABF build-up substrates. They say it is promising as a cost-effective, easy-to-use solution for RDL manufacturing, especially for printed circuit board (PCB) manufacturers that have conventionally used dry film resist, because the new material can be applied using the same processes and equipment. **(Paper 33.2, “*Novel Negative-Tone Dry Film Resist and Process For Fine Pitch Copper Wiring With L/S = 1.5/1.5 µm on Build-Up Substrate*,” K. Togasaki et al, Resonac Corp.)**

**B) Quantum and High-Performance Computing**

**Advanced Packaging Drives Quantum Computing Forward:** Quantum computers may provide efficient solutions to certain problems that are intractable to classical computers. They work by processing quantum bits (qubits) which represent 0, 1 or both at the same time, thanks to their ability to be in the quantum state of “superposition.” Qubits are unstable, with short “coherence times” (how long they can stay in a quantum state). Although multiple qubit technologies exist, superconducting qubits that operate at cryogenic temperatures are one of the most mature approaches. They are lithographically scalable and are transitioning from a lab-scale experiment to commercial products.

However, advanced cryogenic qubit packaging is critical for further progress, because it enables the integration of higher-density qubit chips, more I/O and smaller interconnect pitches, while maintaining coherence and high-fidelity performance. But while standard cryogenic qubit packaging uses a wire bonding approach to route signals from a commercial printed circuit board interposer onto a custom qubit chip, this unfortunately can cause a significant impedance mismatch and electromagnetic energy leakage. MIT Lincoln Laboratory researchers will describe how they designed and demonstrated a reworkable (i.e., resolderable) heterogeneous integration approach for the chip-to-interposer/substrate attachment process. It makes use of microbumps, not wirebonds, to minimize impedance mismatch and crosstalk, by reducing interconnect length. The fact it is reworkable means that it also enables the selective removal and replacement of damaged, non-functional chips. **(Paper #11.1, “*Reworkable Superconducting Qubit Package For Quantum Computing*,” R. Das et al, MIT Lincoln Laboratory)**

**New DC-DC Converter Module for High-Performance Computing:** Voltage-droop is a growing problem as more components are integrated into advanced packages. Murata researchers will describe a novel DC-DC converter module that addresses the issue for high-performance computing (HPC) applications and vertical power delivery packaging architectures. The module has a low profile, good transient response and high efficiency. It makes use of an advanced low-impedance substrate the researchers call integrated Package Solution (iPaS), which has embedded capacitors that are specialized for power delivery.

The researchers demonstrated its performance with modules ≤5 mm in height, which is low enough to be mounted on the backside of the motherboard of an accelerator card for HPC. Using the low-impedance iPaS substrate (1 mΩ @ 1 MHz), nearly the same voltage-droop was achieved vs. that of a general module, even with a >60% reduction of SMD-type capacitors. When the number of SMD capacitors was not reduced, the voltage droop improved by 14 mV (10 %), demonstrating that the technology will be an effective solution for improving the transient response of power supply modules. Power supply efficiency was further improved by more than two points when the researchers added inductors to the space created by reducing the number of SMD-type capacitors. They researchers say this novel technology will be a solution for power supply issues for the next generation of HPC. **(Paper 25.7, “*A Novel DC-DC Converter Module Using the Integrated Package Solution (iPaS) Substrate For Next-Generation High-Performance Computing (HPC) Applications*,” S. Yamada et al, Murata)**

1. **Silicon Photonics**

**World’s First 51.2T Co-Packaged Ethernet Switch for Data Centers:** The tremendous growth in data center traffic has created an urgent need for higher bandwidth and lower power consumption/latency within data centers. A Broadcom-led team will describe the world’s first 51.2T ethernet switch system with co-packaged optics for data center connectivity. It quadruples the bandwidth of widely deployed 12.8 Tbps networking solutions, and leads to a significant reduction in overall power consumption per bit transmitted. It makes use of silicon photonic (SiPh) chiplets co-packaged with silicon switch die on the same substrate, with short interconnects. The researchers built a prototype that co-packaged eight optical engines with switch die, yielding the 51.2 Tbps performance. **(Paper# 3.1, “*High-Density Integration of Silicon Photonic Chiplets For 51.2T Co-Packaged Optics*,” S. Kannan et al, Broadcom/Siliconware Precision Industries Co.**

**D) Reliability and Test**

**Thermocompression Bonding in Large Multichip Modules:** As AI and high-performance computing applications grow in sophistication, the demands for higher bandwidth and faster data transfer rates will only continue to increase. Various semiconductor packaging solutions are being pursued to help meet these demands in multichip module architectures. One of them makes use of small pieces of silicon (Si) containing lines of interconnect, known as silicon bridges, which are used to span physical gaps and to interconnect the chips in multichip modules. ASE researchers will describe a version of this technology called Fan-Out-Chip-on-Substrate-Bridge (FOCoS-Bridge), and how they used it to build and test for the first time a large chip module (>3X Si reticle size) containing 10 chiplets and 10 Si bridge dies. Two versions of this module were built and tested. One had a fan-out size of 31 x 47 mm2 (overall package size = 70 x 78 mm2), and the other, with more complex backside metallization, had a fan-out size of 50 x 50 mm2 (package size = 76.5 x 80 mm2).

An issue with such large sizes is the potential for warpage, caused by differing coefficients of thermal expansion among the Si dies, redistribution layer (RDL), molding layers, copper pillars, Si bridges, microbumps, and organic substrate. The researchers used a thermocompression bonding process to reduce warpage during fabrication, and a variety of inspection methods afterward to evaluate the resulting modules. These included optical microscopy, shadow moiré, x-rays, focused ion beam and scanning electron microscopy. They say the results show that thermocompression bonding is appropriate for large-scale chiplet integration with embedded Si bridges, and is suitable for high-density advanced packaging for high volume manufacturing. **(Paper 23.1, “*Advanced Thermocompression Bonding Application on High-Density Fan-Out Embedded Bridge Technology For HPC/AI/ML*,” W. Wudjud et al, ASE/Advanced Semiconductor Engineering, Inc.)**

**Studying the Reliability of Low-Temperature Solder Joints**: Low-temperature solders (LTSs) are growing in popularity in surface-mount architectures for their lower melting points, which reduce reflow temperatures and minimize warpage, cost and energy consumption. However, failure analyses of joints made with LTSs are ongoing. A team of investigators from Auburn University, NXP Semiconductors and Binghamton University will describe their analyses of hybrid joints consisting of ball grid array (BGA) packages containing Sn-Ag-Cu (SAC) solder balls, mounted onto printed circuit boards (PCBs) with LTS paste. These joints tend to have varying concentrations of bismuth (Bi) from the PCB copper pad to the component’s copper pad. Bi diffusion potentially increases reliability during thermal cycling by restricting the coarsening of intermetallic compound particles/layers. However, excessive Bi concentrations at the PCB side can lead to Bi-embrittlement, making it a prevalent failure location.

The researchers performed creep tests to study solder deformation over time, including a modified Garofalo creep model to account for Bi diffusion in hybrid joints. They also developed a finite element model of a BGA assembly with hybrid joints. The modeling results were correlated with experimental board-level failure data, and the Bi distribution in the joints was modeled across multiple layers. The Bi-concentration gradient in each layer was chosen to replicate observations in the actual joints, which were mapped by energy-dispersive X-ray spectroscopy (EDS). At ECTC, the researchers will describe the results of these studies, and how they can be used to predict PCB-end failure in hybrid joints under various thermal conditions. **(Paper 12.6, “*Analysis of Mechanical Behavior of Hybrid SAC-LTS Joints Under Temperature Cycling With a Modified Garofalo Creep Model Based on Bi Concentration*,” S. Chakraborty et al, Auburn Univ/NXP Semiconductors/Binghamton Univ.)**

**Multiple Testing Techniques Needed to Assess Wafer-to-Wafer Adhesion:** Wafer-to-wafer hybrid bonding enables the integration of heterogeneous wafers with different functionalities and materials, and also enables high interconnection densities. However, hybrid bonding requires a dielectric layer with bonding energy high enough to withstand aggressive processing steps such as grinding, dicing and packaging. Characterizing the bonding strength between the wafers is vital but challenging. It requires reliable and accurate methods that can provide relevant information for optimizing the bonding process and ensuring the reliability of the devices.

IMEC researchers will describe several complementary techniques they used to assess the bonding strength of wafers with silicon carbon nitride (SiCN) as the primary bonding surface. The methods were: a Maszara test, four-point bending, and nanoindentation-based techniques (using wedge and cube corner indenter tips). Because these tests yield similar trends when used in the same interface, the researchers say using them together enables results to be cross-checked for accuracy. For example, in their test devices, in all cases it was observed that the adhesion energy of SiCN/SiCN interfaces increases rapidly at post-bond anneal temperatures of ~200°C, and reaches its maximum at 250°C. **(Paper 19.5, “*Methodologies For Characterization of W2W Bonding Strength*,” M. Gonzalez et al, IMEC)**

**Optimized Modeling Solution to Predict Board Warpage/Localized Stresses:** Higher-performance and lower-power hardware is needed to process fast-growing generative AI (GenAI) workloads such as Large Language Models (LLMs). These devices require more silicon to be integrated into a single package, along with more chip-to-chip interconnects among the packages on a printed circuit board. This means boards are being designed with ever-smaller features, including copper traces with finer lines and spacings, and higher-aspect-ratio vias between metal layers. With these smaller features, identifying key risks such as overall board warpage and localized stress on fine features like traces and vias, is essential to the viability of future hardware.

In this work, Groq expands on using finite element analysis (FEA) simulations to develop a comprehensive modeling solution. This approach can be used to both evaluate and mitigate risks during board assembly. The researchers studied the advantages and drawbacks of three different modeling approaches to understand global warpage behavior – rule-of-mixture, trace mapping, and full reinforcement modeling. They concluded that an optimal modeling methodology requires a hybrid approach to balance accuracy and computational time. Their proposed warpage-modeling methodology has great accuracy against measurement data for risk-location prediction. Groq also will talk about the importance of other issues – part-to-part manufacturing variations, repeatability testing during temperature cycling, and stress-free temperature identification – that can impact board-level warpage predictions. Moreover, Groq’s proposed methodology also reveals high risk locations for millions of fine feature traces and vias embedded in the board, enabling a thorough understanding of board behavior during the assembly process. **(Paper 24.6, “*Optimized Simulation Methodology of Warpage and Localized Stress Hotspot Prediction For Assembly Risk Assessment*,” Z. Yang et al, Groq Inc./Ansys)**

**Building Better BGAs for High-Current, High-Performance Applications:** Current densities for high-performance applications such as AI/ML (artificial intelligence/machine learning) have continued to increase to levels never seen before. The power consumption of modules in the advanced nodes used in these applications is starting to exceed 1 kilowatt, resulting in critical current values throughout the power-delivery path. Because many improvements already have been made to 1st-level interconnect structures (i.e., to copper pillars and to the “C4s” used in flip-chip interconnections), the 2nd-level interconnect – the ball grid arrays (BGAs) which connect packages to circuit boards – is now becoming the weakest link in power delivery, due to electromigration caused by high currents.

To learn how BGA performance can be improved, a collaboration team between Imec and Marvell conducted analyses of the current-carrying capability of BGAs under a variety of different conditions, taking into account substrate design, pad finishes and solder materials, and process variations. They will describe how they used thermal/electrical simulations to guide the design of their experiments, which validated their analyses. They say the work provides confidence that BGA solder ball design rules could be stretched up to 3 A per connection using optimized design and material combinations. **(Paper #16.7, “*BGA Electromigration Behavior and Why it Has Become the Bottleneck*,” R. Labie et al, IMEC/Marvell)**

**Laser-Assisted Bonding for Indium Solder:** As semiconductor components have become smaller, more complex and more highly integrated, there has been a growing emphasis on the issue of heat transfer between them. In particular, micro-LED displays, optoelectronic devices and microelectromechanical systems (MEMS) may have low heat tolerance and may experience degradation at high process temperatures. This means that effective soldering materials and processes are needed to address thermal issues during assembly. Indium solder is one of the most commonly used low-temperature solders, with excellent ductile properties and a low melting point (156.6℃.) It also exhibits superior electrical and thermal conductivity. However, the lack of standardized process parameters for indium soldering means that more research is needed in this area.

To derive the optimal process window, an ETRI-led team established process methods (including bonding techniques, materials, and conditions), and conducted experiments using laser-assisted bonding (LAB) at room temperature vs. traditional thermocompression bonding. The LAB process with indium solder demonstrated effective bonding and good reliability under all conditions with a laser irradiation time of five seconds or more. The findings also suggest that because the LAB process takes place at room-temperature, it reduces overall energy consumption and is attractive for use with heat-sensitive components. **(Session 41, Student Poster Paper, “*Reliability of Indium Solder Joints Using a Laser-Assisted Bonding (LAB) Process at Room Temperature*,” J. Jung et al, ETRI/Hanbat Nat’l Univ.)**

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